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EXAMINER	
FENNEMA, ROBERT E	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 06/08/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/816,103	GROCHOWSKI ET AL.	
	Examiner	Art Unit	
	Robert E. Fennema	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *31 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18,20-28,32-51 and 55-65* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18,20-28,32-51 and 55-65* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *10/14/05; 3/31/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-18, 20-28, 32-51, and 55-65 are pending. Claims 19, 29-31, and 52-54 have been cancelled as per applicants request.

Information Disclosure Statement

2. The IDS filed October 14, 2005 contains two US Patent Application Publications listed on it with invalid numbers. The Application Publications by Cota-Robles and Williams et al. have thus not been considered.

Specification

3. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

4. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 3 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. It is unclear if "a first thread" is supposed to refer to the shred, or a new separate thread, which may be a process, wherein the shred is a thread in said process. Likewise, it is unclear what the difference between "a second shred" and "a second thread" is.

Claim Objections

7. Claim 44 refers to "the multiprocessor"; however, no multiprocessor has been introduced in this claim or the independent claim.

8. Claim 61 refers to a "said prioritizer" from Claim 33, but no prioritizer has been introduced in Claim 33. It is believed that Claim 61 is meant to depend from Claim 34, and has been assumed as such for the remainder of the Office Action.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

10. Claims 17-18, 20-28, 32, 35-44, 55-58, and 62 are rejected under 35 U.S.C. 102(b) as being anticipated by Lawlor et al. (USPN 5,485,626, herein Lawlor).

11. As per Claim 17, Lawlor teaches: An apparatus, comprising:

execution resources to execute a plurality of instructions (Column 10, Lines 47 and 51, the processors),

the execution resources including multiple instruction sequencers (Column 11, Line 28, each processor has an Instruction control unit);

the execution resources to receive a non-privileged user instruction (Column 8, Lines 37-42. Furthermore, the disclosed invention is geared towards not using the operating system (Abstract and Column 6, Lines 38-42), meaning that these instructions would be non-privileged); the execution resources further to, responsive to the received instruction, begin execution of a shred concurrently with one or more other shreds (Column 12, Lines 31-32).

12. As per Claim 18, Lawlor teaches: The apparatus of claim 17, further comprising:

one or more shared shred registers to facilitate communication between two or more of the shreds (Column 19, Lines 31-32).

13. As per Claim 20, Lawlor teaches the apparatus of claim 18, wherein the one or more shared registers further comprise a first register that enables an operating system or BIOS to enable multithreading architecture extensions for user-level multithreading (Column 18, Lines 13-19).

14. As per Claim 21, Lawlor teaches: The apparatus of claim 17, wherein the execution resources are further to, responsive to the received instruction, begin execution of a shred concurrently with one or more other shreds, without control of an operating system (Column 12, Lines 31-32).

15. As per Claim 22, Lawlor teaches: The apparatus of claim 17, wherein the execution resources include one or more processor cores capable of executing multiple shreds concurrently (Column 10, Lines 47 and 51).

16. As per Claim 23, Lawlor teaches: The apparatus of claim 17, further comprising:

One or more registers to hold a state shared among the shred and the one or more other shreds (Column 8, Lines 20-24, they share an object space containing counters and queues, which can be implemented in registers as seen in Column 8, Lines 59-60).

17. As per Claim 24, Lawlor teaches: The apparatus of claim 17, wherein the shred and the one or more other shreds share a current privilege level and share a common address translation (Column 8, Lines 37-42 show that the compiler creates instructions to create parallelism (threads/shreds) outside of the operating system, giving them the same privilege level (non privileged) as the others. In addition, Column 8, Lines 20-23 discusses the addressing).

18. As per Claim 25, Lawlor teaches: The apparatus of claim 17, further comprising logic to execute a user-level instruction to create the shred (Column 8, Lines 37-42).

19. As per Claim 26, Lawlor teaches: The apparatus of claim 17, further comprising a mechanism to perform communication between the shred and the one or more other (Column 17, Lines 13-18).

20. As per Claim 27, Lawlor teaches: The apparatus of claim 17, further comprising sharing a system state among the shred and the one or more other shreds (Column 8, Lines 20-28).

21. As per Claim 28, Lawlor teaches: The apparatus of claim 26, wherein the mechanism further comprises one or more shared registers (Column 19, Lines 31-32).

22. As per Claim 32, Lawlor teaches: The apparatus of claim 17, further comprising:

a user-level exception mechanism to report an exception to the shred (Column 18, Lines 21-22).

23. As per Claim 35, Lawlor teaches: An article of manufacture, comprising:

a machine-accessible medium including data that, when accessed by a machine, cause the machine to perform operations comprising,

receiving user-level programming instructions to execute a plurality of shared resource threads (shreds) (Column 8, Lines 37-42);

configuring one or more instruction sequencers responsive to the one or more user-level programming instructions (Column 11, Lines 40-42);

scheduling the shreds via hardware (Column 12, Lines 50-52); and

executing the plurality of shreds concurrently on multiple instruction sequencers (Column 12, Lines 31-32).

24. As per Claim 36, Lawlor teaches: The article of manufacture of claim 35, wherein the operations further comprise:

maintaining a private state for each shred of the plurality of shreds, wherein the private state is associated with at least one of a plurality of registers including general purpose registers, floating point registers, MMX registers, segment registers, a flags register, an instruction pointer, control and status registers, SSE registers, and a MXCSR register (Column 18, Lines 14-18).

25. As per Claim 37, Lawlor teaches: The article of manufacture of claim 35, wherein the machine-accessible medium further includes data that causes the machine to perform operations comprising sharing a first state among the plurality of shreds, while maintaining a second state privately among an additional shred associated with a thread that is not associated with the plurality of shreds, wherein the first state is associated with at least one of a plurality of registers including a control register, a flags

register, memory management registers, a local descriptor table register, a task register, debug registers, model specific registers, shared registers, and shred control registers (Column 11, Lines 3-5 show the program context is stored in the SV register 112).

26. As per Claim 38, Lawlor teaches: The article of manufacture of claim 35, wherein the machine-accessible medium further includes data that causes the machine to perform operations comprising:

sharing a state among the plurality of shreds; and storing the state in one or more registers (Column 8, Lines 20-24, they share an object space containing counters and queues, which can be implemented in registers as seen in Column 8, Lines 59-60).

27. As per Claim 39, Lawlor teaches: The article of manufacture of claim 35, wherein the plurality of shreds share a current privilege level and share a common address translation (Column 8, Lines 37-42 show that the compiler creates instructions to create parallelism (threads/shreds) outside of the operating system, giving them the same privilege level (non privileged) as the others. In addition, Column 8, Lines 20-23 discusses the addressing).

28. As per Claim 40, Lawlor teaches: The article of manufacture of claim 35, wherein the one or more user-level programming instructions include an instruction to create one

or more of the plurality of shreds (Column 8, Lines 37-42).

29. As per Claim 41, Lawlor teaches: The article of manufacture of claim 35, wherein the machine-accessible medium further includes data that causes the machine to perform operations comprising communicating among the plurality of shreds (Column 17, Lines 13-18).

30. As per Claim 42, Lawlor teaches: The article of manufacture of claim 35, wherein the machine-accessible medium further includes data that causes the machine to perform operations comprising sharing a system state among the plurality of shreds (Column 8, Lines 20-28).

31. As per Claim 43, Lawlor teaches: The article of manufacture of claim 35, wherein the machine-accessible medium further includes data that causes the machine to perform operations comprising communicating between the plurality of shreds via one or more shared registers (Column 19, Lines 31-32).

32. As per Claim 44, Lawlor teaches: The article of manufacture of claim 35, wherein an application program controls the plurality of shreds directly, including scheduling of the plurality of shreds, and wherein an operating system executed by the multiprocessor schedules one or more threads (Column 2, Lines 21-31).

33. As per Claim 50, Lawlor teaches: The article of manufacture of claim 35, wherein the plurality of shreds perform input/output (I/O) functions and computation functions (Column 12, Lines 31-41).

34. As per Claim 55, Lawlor teaches: A system, comprising:

a microprocessor (Column 10, Line 58, Processor 106), including a plurality of user-level multithreading registers coupled to the microprocessor (Column 19, Lines 31-32); and

memory coupled to the microprocessor (Column 11, Lines 44-46) that stores an instruction set architecture (ISA) compatible with the microprocessor and the plurality of user-level multithreading registers (Column 7, Lines 1-4), wherein the memory is from a plurality of memory devices including DRAM, flash, and EEPROM (Column 11, Lines 44-46),

wherein the plurality of user-level multithreading registers and the ISA enable multithreading architecture extensions for user-level multithreading (Column 7, Lines 1-4).

35. As per Claim 56, Lawlor teaches: The system of claim 55, wherein the plurality of user-level multithreading registers further comprises a plurality of shared shred registers to facilitate communication between a plurality of shreds and to facilitate synchronization between the plurality of shreds (Column 19, Lines 31-32).

36. As per Claim 57, Lawlor teaches: The system of claim 56, wherein the plurality of user-level multithreading registers further comprises a plurality of shred control registers to manage the plurality of shreds (Column 18, Lines 13-18).

37. As per Claim 58, Lawlor teaches The system of claim 57, wherein the microprocessor:

receives programming instructions to execute one or more shreds in accordance with the ISA (Column 8, Lines 37-42);

configures one or more instruction sequencers via the ISA (Column 11, Lines 40-42); and

executes the one or more shreds concurrently (Column 12, Lines 31-32).

38. As per Claim 62, Lawlor teaches: The article of manufacture of claim 35, wherein the one or more user-level programming instructions include an instruction to destroy one or more of the plurality of shreds (Column 29, Lines 27, 49, and Column 30, Line 4).

Claim Rejections - 35 USC § 103

39. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

40. Claims 1-12,15-16, and 45-46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lawlor, in view of Foldoc.

41. As per Claim 1, Lawlor teaches: A method, comprising:

encountering a non-privileged user-level programming instruction (Column 8, Lines 37-42. Furthermore, the disclosed invention is geared towards not using the operating system (see Column 4, Lines 20-24 and Abstract), meaning that these instructions would be non-privileged, as seen in the Foldoc articles "privileged instruction" and "supervisor mode");

creating, responsive to the programming instruction, a first shared resource thread (shred) (Column 8, Lines 37-42, and Column 24, Line 36 as an example of a thread creation instruction); and

executing, responsive to the programming instruction, the shred concurrently with at least one of the one or more other shreds (Column 12, Lines 31-32);

wherein creating the shred is performed in hardware, without the intervention of an operating system (Abstract and Column 6, Lines 38-42), but fails to teach:

the shred sharing virtual memory address space with one or more other shreds.

While Lawlor teaches that users have access to a certain amount of address space (Column 8, Lines 20-27), and that the operating system can define what address spaces those are, Lawlor therefore teaches that multiple shreds could share the same address space, if the OS configured it in that way. However, Lawlor does not teach that this is virtual memory address space. However, Foldoc (see "virtual memory" article)

teaches that virtual memory is a system used to trick systems into being able to address more memory than is actually in the physical RAM, allowing programs larger than the RAM size to run (Paragraph 1). In addition, the "demand paged" virtual memory allows multiple programs to be loaded into the RAM at once, perfect for a multitasking environment such as Lawlor's (Paragraph 4). Using virtual memory in a computing system is well known in the art, exemplified by Foldoc, and thus would have been obvious to one of ordinary skill in the art at the time the invention was made to include in any computer system utilizing Lawlor's invention.

42. As per Claim 2, Lawlor teaches: The method of claim 1, further comprising:

Maintaining a private state for the first thread, wherein the private state is associated with at least one of a plurality of registers including general purpose registers, floating point registers, MMX registers, segment registers, a flags register, an instruction pointer, control and status registers, SSE registers, and a MXCSR register (Column 18, Lines 14-18).

43. As per Claim 3, Lawlor teaches: The method of claim 1, further comprising:

sharing a state among a plurality of shreds associated with a first thread, the plurality of shreds including the first shred and the one or more other shreds; while not sharing said state with a second shred that is associated with a second thread (Since it is unclear what the applicant intended to mean by "a first thread", it has been interpreted to mean a process from which shreds are created from. Column 11, Lines 3-5 show this

context is stored in the SV register 112).

44. As per Claim 4, Lawlor teaches: The method of claim 1, further comprising:

sharing a state among a plurality of shreds of the one or more shreds; and storing the state in one or more registers (Column 8, Lines 20-24, they share an object space containing counters and queues, which can be implemented in registers as seen in Column 8, Lines 59-60).

45. As per Claim 5, Lawlor teaches: The method of claim 1, wherein the first shred and the one or more shreds share a current privilege level and share a common address translation (Column 8, Lines 37-42 show that the compiler creates instructions to create parallelism (threads/shreds) outside of the operating system, giving them the same privilege level (non privileged) as the others. In addition, Column 8, Lines 20-23 discusses the addressing).

46. As per Claim 6, Lawlor teaches: The method of claim 1, further comprising:

receiving a non-privileged user-level programming instruction that encodes a shred destroy operation (Column 29, Lines 27, 49, and Column 30, Line 4).

47. As per Claim 7, Lawlor teaches: The method of claim 1, further comprising communicating between the first shred and at least one of the one or more other shreds

(Column 17, Lines 13-18).

48. As per Claim 8, Lawlor teaches: The method of claim 1, further comprising sharing a system state among the one or more shreds (Column 8, Lines 20-28).

49. As per Claim 9, Lawlor teaches: The method of claim 7, wherein said communicating is performed via one or more shared registers (Column 19, Lines 31-32).

50. As per Claim 10, Lawlor teaches: The method of claim 1, further comprising:

scheduling, responsive to a user-level programming instruction, the first shred and the one or more other shreds without intervention of the operating system (Column 7, Lines 37-42).

51. As per Claim 11, Lawlor teaches: The method of claim 7, wherein:

said communicating is performed via a user-level shred signaling instruction (Column 17, Lines 13-18).

52. As per Claim 12, Lawlor teaches: The method of claim 11, further comprising:

storing one or more shred states associated with the one or more shreds responsive to receipt of a context switch request (Column 18, Lines 14-18).

53. As per Claim 15, Lawlor teaches: The method of claim 1, wherein:

The shred is to perform input/output (I/O) operations (Column 12, Lines 35-41).

54. As per Claim 16, Lawlor teaches: The method of claim 1, wherein:

the one or more shreds are to perform computation functions (Column 12, Lines 31-32).

55. As per Claim 45, Lawlor teaches: The article of manufacture of claim 35, wherein the machine-accessible medium further includes data that causes the machine to perform operations comprising:

associating the plurality of shreds with a thread (Column 8, Lines 20-24, by creating threads to increase parallelism, this is the same as making threads for a process as shown by Foldoc "Process"), but fails to teach:

suspending the plurality of shreds belonging to the thread when a context switch request is received through a single one of the plurality of shreds. In Column 18, Lines 13-18, Lawlor teaches that the context is saved when a thread goes inactive, but does not teach that all threads/shreds of a process would be made to be suspended on a context switch. However, Foldoc (Context switch) teaches that on a context switch between processes, the entire process stops running, and another begins. Given that the reason to multithread (See Foldoc, "multithreading") is to maximize the shared state as much as possible, it would have been obvious to one of ordinary skill in the art at the time the invention was made to shut down all the shreds associated with the

thread/process when it was switched out, so the new process could make use of the advantages of parallelism without the other shreds getting in the way.

56. As per Claim 46, Lawlor teaches: The article of manufacture of claim 45, wherein the machine-accessible medium further includes data that causes the machine to perform operations comprising:

storing one or more shred states associated with the plurality of shreds when the context switch request is received (Column 18, Lines 13-18).

57. Claims 13-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lawlor and Foldoc, further in view of Golliver et al. (USPN 6,378,067, herein Golliver).

58. As per Claim 13, Lawlor teaches the method of claim 1, but fails to teach:

handling with user-level exception handler code an exception generated during execution of the first shred, without intervention of the operating system.

Lawlor teaches that exceptions can be generated and are dealt with (Column 18, Lines 21-22 for example), but does not explicitly disclose how this occurs, or what deals with the exceptions. Golliver teaches a method to handle multiple exceptions at once by prioritizing them, and dealing with them in a non-operating system exception handler (Column 3, Line 66 – Column 4, Line 6, and Column 4, Lines 22-25. The operating system is not used to process the exception unless explicitly called, as shown in Column 7, Lines 22-27). Given the need for a method to handle exceptions, and the

desire to minimize the operating systems involvement in thread processing in Lawlor's invention, and additionally the need to handle multiple exceptions which could come up when executing multiple shreds concurrently, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use Golliver's exception handler to handle Lawlor's exceptions.

59. As per Claim 14, Golliver teaches: The method of claim 13, further comprising:

receiving the exception from an application program (Column 4, Lines 22-26); and

determining whether to report the exception to the operating system (Column 7, Lines 25-27).

60. Claims 33-34, 47-49 and 59-61 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lawlor, in view of Golliver.

61. As per Claim 33, Lawlor teaches the apparatus of claim 17, but fails to teach:

an exception mechanism to report an exception to an operating system.

Lawlor teaches that exceptions can be generated and are dealt with (Column 18, Lines 21-22 for example), but does not explicitly disclose how this occurs, or what deals with the exceptions. Golliver teaches a method to handle multiple exceptions at once by prioritizing them, and dealing with them in a non-operating system exception handler (Column 3, Line 66 – Column 4, Line 6, and Column 4, Lines 22-25. The operating

system is not used to process the exception unless explicitly called, as shown in Column 7, Lines 22-27). Given the need for a method to handle exceptions, and the desire to minimize the operating systems involvement in thread processing in Lawlor's invention (but still be able to use it when necessary), and additionally the need to handle multiple exceptions which could come up when executing multiple shreds concurrently, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use Golliver's exception handler to handle Lawlor's exceptions.

62. As per Claim 34, Golliver teaches: The apparatus of claim 32, further comprising:

a mechanism to detect multiple exceptions, each exception associated with a different one of a plurality of concurrently-executing shreds, where the plurality includes the shred and the one or more other shreds (Column 3, Line 66 – Column 4, Line 6, and Column 5, Lines 29-31);

wherein the exception mechanism includes a prioritizer to prioritize the exceptions (Column 4, Line 1); and

wherein the exception mechanism is further to report only one of the prioritized exceptions at a time to the operating system (Column 7, Lines 23-28 disclose the operating system may be able to be told to handle exceptions, and Column 7, Lines 11-13 show that the faults can be reported one at a time).

63. As per Claim 47, Lawlor teaches the article of manufacture of claim 35, but fails to teach:

wherein the machine-accessible medium further includes data that causes the machine to perform operations comprising:

reporting one or more exceptions to a first shred of the plurality of shreds.

Lawlor teaches exceptions occurring (Column 18 Lines 20-21 for example), but does not teach explicitly what happens during an exception. Golliver teaches a method to handle multiple exceptions at once by prioritizing them, and reporting them to a non-operating system exception handler (Column 3, Line 66 – Column 4, Line 6, and Column 4, Lines 22-25. The operating system is not used to process the exception unless explicitly called, as shown in Column 7, Lines 22-27). Given the need for a method to handle exceptions, and the desire to minimize the operating systems involvement in thread processing in Lawlor's invention (but still be able to use it when necessary), and additionally the need to handle multiple exceptions which could come up when executing multiple shreds concurrently, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use Golliver's exception handler to handle Lawlor's exceptions.

64. As per Claim 48, Golliver teaches: The article of manufacture of claim 47, wherein the machine-accessible medium further includes data that causes the machine to perform operations comprising:

reporting the one or more exceptions from an application program (Column 2, Lines 42-47); and

determining whether to report the one or more exceptions to an operating system (Column 7, Lines 23-27).

65. As per Claim 49, Golliver teaches: The article of manufacture of claim 48, wherein the machine-accessible medium further includes data that causes the machine to perform operations comprising:

prioritized-reporting of the one or more exceptions to the operating system; comprising receiving the one or more exceptions concurrently via different shreds of the plurality of shreds (Column 5, Lines 30-32); and

servicing one of the one or more exceptions according to the prioritized-reporting while suspending exception processing of other exceptions of the one or more exceptions (Column 7, Lines 11-13).

66. As per Claim 59, Golliver teaches: The apparatus of claim 32, wherein: the user-level exception mechanism is further to vector to a fixed location in order to allow the shred to service to the exception (Figure 4, and Column 7, Lines 23-28, the user handler set).

67. As per Claim 60, Golliver teaches: The apparatus of claim 32, wherein:

the plurality of instructions further include a system call instruction to explicitly invoke an operating system to service to the exception (Column 7, Lines 23-28).

68. As per Claim 61, Golliver teaches: The apparatus of claim 33, wherein said prioritizer employs a round-robin scheme (Column 7, Lines 11-12 and Column 5, Lines 30-32).

69. Claims 51 and 63-65 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lawlor, in view of Patterson et al. (herein Patterson).

70. As per Claim 51, Lawlor teaches: A system, comprising:

a microprocessor implementing an instruction set architecture (ISA) (Column 7, Lines 1-4); and

a memory (Figure 2, Memory 211 and cache 201); wherein the ISA includes one or more instructions to allow user-level multithreading operations (Column 7, Lines 1-4), but fails to teach:

the microprocessor capable of executing multiple concurrent shreds.

Lawlor teaches a multiprocessor system, where each processor is capable of working on a single shred at a time, but does not teach that each individual processor is capable of executing more than one shred at a time. However, Patterson teaches a system of increasing parallelism and increasing performance by making a processor superscalar (Page 215). Instructions that do not depend on each other (i.e.,

independent instructions that can be run in parallel, just like shreds) can be issued simultaneously (Pages 216-217). Given this advantage, and the statement by Lawlor which says that being able to dynamically assign processors to increase the processing time of the job is favorable (Column 8, Lines 50-58), it would have been obvious to one of ordinary skill in the art at the time the invention was made to consider making Lawlor's processors superscalar, to further increase the parallelism of the shred processing.

71. As per Claim 63, Lawlor teaches: The system of claim 51, wherein the one or more instructions include an instruction to create a shred without intervention of an operating system (Column 4, Lines 20-23).

72. As per Claim 64, Lawlor teaches: The system of claim 51, wherein the one or more instructions include an instruction to destroy a shred without intervention of an operating system (Column 29, Lines 27, 49, and Column 30, Line 4).

73. As per Claim 65, Lawlor teaches: The system of claim 51, wherein: the user-level multi-threading operations include concurrent execution of two or more shreds associated with the same thread (Column 4, Lines 10-15, where it says that a shred (fork) is created when a part of the program is found to be able to be executed in parallel, thus all the shreds are threads of an overall process (the thread in this case)).

Conclusion

74. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

75. Levy et al. (USPN 6,092,175) teaches a multithreading system with shared and private registers.

76. Kiefer et al. (USPN 6,223,208) teaches a multithreading system.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Robert E. Fennema whose telephone number is (571) 272-2748. The examiner can normally be reached on Monday-Friday, 8:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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